A new Square-Root Circuit Using Short Channel MOSFETs with Compensation for Error Resulting from Carrier Mobility Reduction

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Abstract—This paper presents a new current-mode square rooter circuit using 0.18μm CMOS technology. The design is based on MOSFETs translinear principle in strong inversion and minimizes the second order effects caused by carrier mobility reduction in short channel MOSFETs. Tanner simulation tool is used to confirm the functionality of the design.

Index Terms—short channel MOSFETs, second order effects, carrier mobility reduction, square root

I. INTRODUCTION

As the transistor is scaled down, second order effects become more important and require modifications to the MOS models or a way to compensate for the errors due to these effects. The main effects that can be compensated for are the channel length modulation, body effect and the carrier mobility reduction. At large gate-source voltage, the high electric field developed between the gate and the channel confines the charge carrier to a narrower region below the oxide-silicon interface, leading to more carrier scattering and hence lower mobility. Since scaling has substantially deviated from the constant-field scenario, small-geometry devices experience significant mobility degradation.

Many compensation techniques in OTA based circuits are reported in the literature [1-5]. There is no much done to compensate for the error generated by the carrier mobility reduction in the current-mode circuits employing MOS trans-linear loop. Reference [6] proposed a technique to reduce the error of the output current caused by mobility reduction. The drawbacks to this circuit are that, this method needs a control voltage to work properly. Also, changes in VDS of this transistor cause variations in the resistance value which can affect the functionality of the circuit. In [7] a squarer/divider circuit is proposed considering second order effects caused by carrier mobility reduction. This design is has a higher precision and smaller chip area. The drawbacks of this design are the use of resistor to compensate for the errors of the voltage term that is added to the MTL loop and this will increase the silicon area of the circuit. A novel higher precision square-root circuit was proposed in [8]. The design suffers from the errors caused by carrier mobility reduction.

In this work, a new approach to compensate for the errors due to carrier mobility reduction in square root circuit employing MOSFETs Translinear Loop (MTL) is proposed. In section II, the proposed circuit is presented. Simulation results and discussion are presented in section III. Section IV concludes the paper.

II. PROPOSED CIRCUIT

The proposed square root circuit diagram is shown in Figure 1. With reference to the figure, the input can be applied via M6 as \( I_x \) or via M9 as \( I_y \). If the input current is negative, use \( I_x \) as the input and \( I_y \) as a bias current and vice versa.

Using MTL in transistors M1, M2, M3 and M4 to get:

\[
I_x + I_y = I_{S3} + I_{S4} \quad (1)
\]

If the mobility reduction is taken into consideration, the MOS drain current is given by:

\[
I_D = \frac{\beta \mu_0}{2} \left( \frac{V_{GS} - V_{TH}}{1 + \theta (V_{GS} - V_{TH})} \right)^2 \quad (2)
\]

Where, \( \theta \) is a fitting parameter and \( \beta \) is the aspect ratio of transistor.

The gate-to-source potential can be written as:

\[
V_{GS} = \frac{I_D \theta}{\beta} + \sqrt{\frac{2I_D}{\beta} + V_{TH}} \quad (3)
\]
Combining Eq (1) and (3) to get:

\[
\frac{I_{D_1}^\beta}{\beta_1} + \frac{2I_{D_1}}{\beta_2} + \frac{I_{D_2}^\beta}{\beta_3} + \frac{2I_{D_2}}{\beta_4} + \frac{2I_{D_3}^\beta}{\beta_5} + \frac{I_{D_3}}{\beta_6} + \frac{2I_{D_4}^\beta}{\beta_7} + \frac{2I_{D_4}}{\beta_8} + \frac{2I_{D_5}^\beta}{\beta_9} + \frac{2I_{D_5}}{\beta_10}
\]

(4)

Where \( I_{D_1} \) is the drain current for the transistor. Assuming that \( \beta_1 = \beta_2 = \beta \) and \( \beta_3 = \beta_4 = 2\beta \) and \( \beta_9 = 2\beta \), then Eq. 4 can be written as:

\[
\frac{I_{x}^\beta}{\beta} + \frac{2I_{x}}{\beta} + \frac{I_{y}^\beta}{\beta} + \frac{2I_{y}}{\beta} + \frac{2I_{x}^\beta}{\beta} + \frac{I_{x}}{\beta} + \frac{2I_{y}^\beta}{\beta} + \frac{2I_{y}}{\beta}
\]

(5)

Since the drain current of transistors M3 and M4 are the same, Eq. 5 can be expressed by:

\[
\frac{\theta}{2\beta} [I_{x} + I_{y}] = \frac{\theta}{\sqrt{2\beta}} [2I_{D_3}]
\]

(6)

If we force the following condition

\[
\frac{\theta}{\beta} [I_{x} + I_{y}] = \frac{\theta}{2\beta} [2I_{D_3}]
\]

(7)

Combining Eq. 6 and 7 to get:

\[
\frac{1}{\sqrt{\beta}} \sqrt{2I_{x} + 2I_{y}} = \frac{1}{\sqrt{\beta}} \sqrt{2I_{D_3}}
\]

(8)

Squaring both side of Eq. 8, then

\[
2[I_{x} + I_{y}] + 4\sqrt{I_{x} \ast I_{y}} = 4I_{D_3}
\]

(9)

Eq. 9 can be written as:

\[
I_{D_3} = \frac{I_{x} + I_{y}}{2} + \sqrt{I_{x} \ast I_{y}}
\]

(10)

Subtracting the term \( \frac{I_{x} + I_{y}}{2} \) from Eq. 10, the output current can be expressed as:

\[
I_{out} = \sqrt{I_{x} \ast I_{y}}
\]

(11)

With reference to Figure 1, the circuit can be used to produce the square root of the current going out, using \( I_{x} \) as input or going in using \( I_{y} \) as an input.

If the current \( I_{y} \) is kept fixed, Eq. 11 can be written as

\[
I_{out} = K\sqrt{I_{x}}
\]

(12)

It is clear that Eq. 12 implements square root circuit.

III. SIMULATION RESULTS

The proposed circuit was simulated using Tanner tools in 0.18µm CMOS technology. The circuit is operating form 1.3V power supply. The aspect ratio of all transistors used for simulation is listed in Table 1. The input current \( I_{y} = 5\mu A \) and \( I_{x} \) is swept from 0 to 20µA. It is clear from the plot that simulated and calculated results are in a good agreement.

<table>
<thead>
<tr>
<th>Table I. Transistor Aspect Ratios</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/L (µm)</td>
</tr>
<tr>
<td>M1 2/0.18</td>
</tr>
<tr>
<td>M2 2/0.18</td>
</tr>
<tr>
<td>M3 4/0.18</td>
</tr>
<tr>
<td>M4 4/0.18</td>
</tr>
<tr>
<td>M5 2/0.18</td>
</tr>
<tr>
<td>M6 2/0.18</td>
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</tbody>
</table>

Simulation and calculated results are shown in Figure 2. It is clear from the plot that simulated and calculated results are in a good agreement.
Figure 2. Simulated and calculated results for the square root circuit.

A. Temperature and Mismatch Analysis

The circuit was simulated for temperature variation. The temperature was varied from 25 to 75°C.

Figure 3. Simulation results for temperature variation.

Simulation against mismatch in channel length was carried out for MOSFETS forming the translinear loop. Simulation result is shown in Figure 4. It is evident from the figure that the variation is in acceptable range.

Figure 4. Simulation result for mismatch analysis.

IV. CONCLUSION

A new square rooter circuit using short channel MOSFETs in strong inversion is developed. The circuit is based on MTL with mobility carrier reduction is minimized. The functionality of the proposed circuit was confirmed using Tanner simulation tool.

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REFERENCES


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